METHOD OF DESIGNING CIRCUIT HAVING MULTIPLE TEST ACCESS PORTS, CIRCUIT PRODUCED THEREBY AND METHOD OF USING SAME

ABSTRACT OF THE DISCLOSURE

5   In a circuit with multiple Test Access Port (TAP) interfaces, the TAPs are arranged into groups, with secondary TAPs in one or more groups and a master TAP in another group, the master TAP having an instruction register with bits for storing a group selection code; a Test Data Output (TDO) circuit responsive to the group selection code connects the group TDO of one of the groups to the circuit

10   TDO; and, for each secondary TAP group, a group Test Data Input (TDI) circuit responsive to a shift state signal for selectively connecting the group TDI to the circuit TDI or to the output of a padding register having its input connected to the circuit TDI, and its output connected to an input of the group TDI circuit; and a group TMS circuit responsive to a predetermined TAP selection code associated with the

15   group for producing a group TMS signal for each TAP in the group.